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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,410	06/01/2006	Daisuke Kumaki	0553-0504	3756

26568 7590 09/29/2009

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EXAMINER	
BOWMAN, MARY ELLEN	
ART UNIT	PAPER NUMBER
2879	

MAIL DATE	DELIVERY MODE
09/29/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,410	KUMAKI ET AL.	
	Examiner	Art Unit	
	MARY ELLEN BOWMAN	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-20 and 32-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-20 and 32-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 5, 2009 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 9-20 and 32-47 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

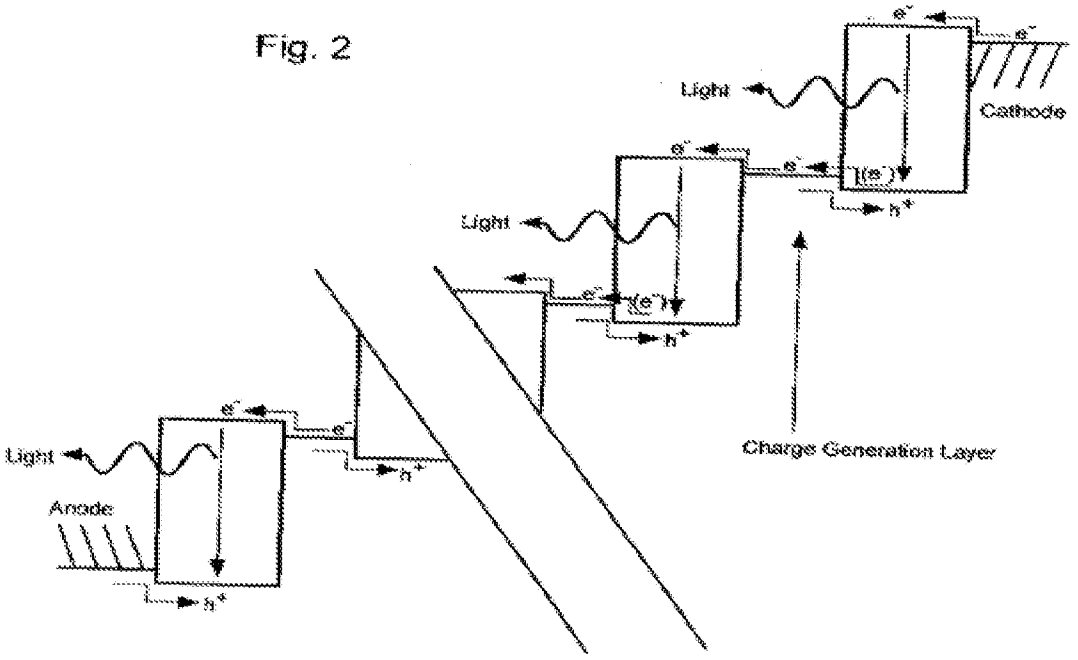
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-20 and 32-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kido et al., USP App. Pub. No. 2003/0189401 A1, published October 9, 2003 (hereinafter referred to as "Kido") in view of Nakaya et al., USP App. Pub. No. 2004/0234814 A1, published November 25, 2004 (hereinafter referred to as "Nakaya").

Regarding claim 9, Kido discloses **a light emitting element comprising: a first electrode and a second electrode** (e.g., Fig. 2 above, anode and cathode)**; a first layer generating holes** ([0028]; "it is desirable for the charge generation layer to include a laminated

and/or a mixed layer including an organic compound having…a hole transporting property [i.e., hole generating layer]...and an inorganic...material"**); a third layer containing a light emitting material** (e.g., Figure 2, light emitting layer)**; and a fourth layer generating electrons** (e.g., [0041]; "an electron injection layer having a mixture including an organic compound and a metal functioning as an electron donating dopant")**.**

Fig. 2



Regarding claim 13, Kido discloses **a light emitting element comprising: a first electrode and a second electrode** (e.g., Fig. 2 above, cathode and anode)**; a first layer containing a P-type semiconductor** ([0028]; "it is desirable for the charge generation layer to include a laminated and/or a mixed layer including an organic compound having…a hole transporting property [i.e., P-type semiconductor]...and an inorganic...material"**); a third layer containing a light emitting material** (e.g., Figure 2, light emitting layer)**; and a fourth layer**

containing an N-type semiconductor (e.g., [0041]; "an electron injection layer having a mixture including an organic compound and a metal functioning as an electron donating dopant [i.e., N-type semiconductor]")**.**

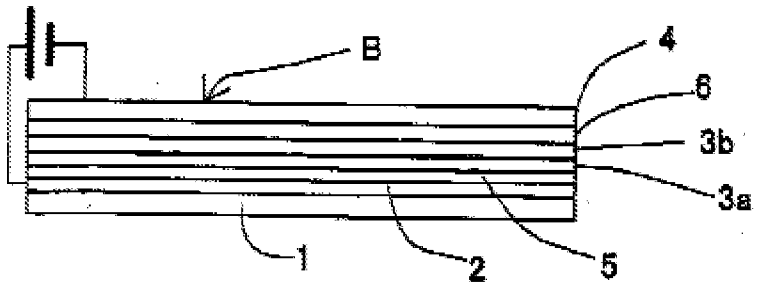
Regarding claim 34, Kido discloses **a light emitting element comprising: a first electrode over a substrate** (e.g., Fig. 2 above, anode over substrate, [0057])**; a first layer generating holes over and in contact with the first electrode** ([0028]; "it is desirable for the charge generation layer to include a laminated and/or a mixed layer including an organic compound having…a hole transporting property [i.e., hole generating layer]...and an inorganic...material [i.e., which accepts the electrons of the organic material]")**; a third layer containing a light emitting material over the first layer** (e.g., Figure 2, light emitting layer)**; a fourth layer generating electrons over the third layer** (e.g., [0041]; "an electron injection layer having a mixture including an organic compound and a metal functioning as an electron donating dopant")**; and a second electrode** (cathode).

Regarding claim 39, Kido discloses **a light emitting element comprising: a first electrode over a substrate** (e.g., Fig. 2 above, anode over substrate, [0057])**; a first layer containing a P-type semiconductor over and in contact with the first electrode** ([0028]; "it is desirable for the charge generation layer to include a laminated and/or a mixed layer including an organic compound having…a hole transporting property [i.e., P-type semiconductor]...and an inorganic...material"; Note: each of the layers is either directly or indirectly contacting the other layers of the device because there are no gaps between the layers)**; a third layer containing a light emitting material over the first layer** (e.g., Figure 2, light emitting layer)**; a fourth layer containing an N-type semiconductor over the third layer** (e.g., [0041]; "an electron injection

layer having a mixture including an organic compound and a metal functioning as an electron donating dopant [i.e., N-type semiconductor]"), **a second electrode** (e.g., cathode).

Regarding claims 9, 13, 34 and 39, Kido fails to teach a second hole generating layer in contact with the cathode. However, in the same field of endeavor of EL displays, Nakaya teaches **a second layer generating holes (and containing a P-type semiconductor)** ([0240-0241]), **wherein the first layer is in direct contact with the first electrode** (layer 5 in direct contact with electrode 2, Figure 2), **the second layer is in direct contact with the second electrode** ([0240-0241]), **the third layer is provided between the first electrode and the second electrode with the first layer and the second layer respectively therebetween** (layers 3a and 3b, Figure 2), **and the fourth layer is provided between the third layer and the second layer** (layer 6, Figure 2 and [0240-0241]).

Figure 2



It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a second hole injection layer on the cathode side of the device, as taught by Nakaya, because said layer can serve as a buffer layer between the light emitting layer and the cathode, thereby lowering the driving voltage of the device (Nakaya; [0241]).

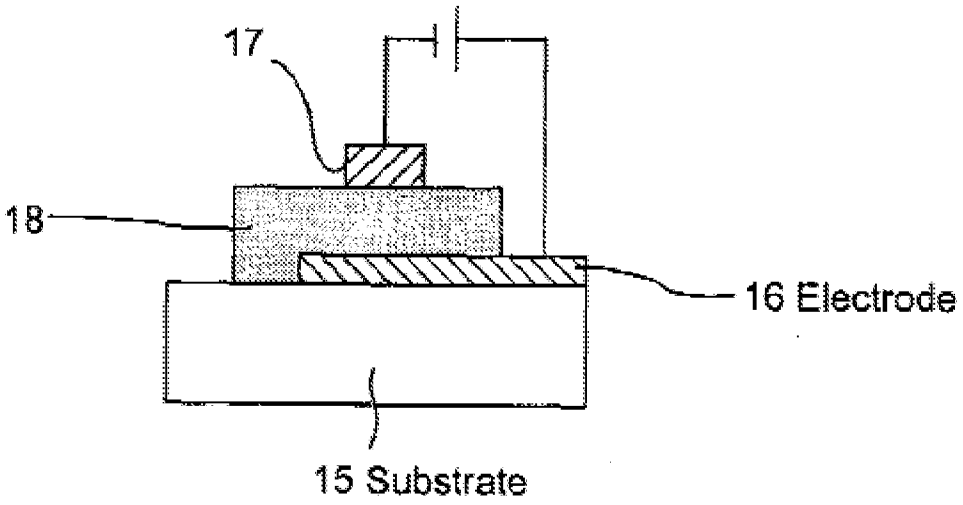
Regarding claims 10, 18, 35 and 44, Kido and Nakaya disclose the inventions as explained above regarding claims 9, 13, 34 and 39 respectively, and Kido further discloses **the**

thickness of each of the first layer and the second layer is 30 nm to 1 μm (e.g., [0052]; "a hole injection layer including an electron accepting compound and having a thickness of not more than 30 nm [i.e., including 30 nm, which is within the claimed range]"; see also Figure 2, there are two hole transporting layers, one on either side of the light emitting layer)**.**

Regarding claims 11, 19, 36 and 45, Kido and Nakaya disclose the inventions as explained above regarding claims 9, 13, 34 and 39 respectively, and Kido further discloses **the thickness of the second layer is 50% to 150% of the thickness of the first layer, and the thickness of the first layer is 50% to 150% of the thickness of the second layer** (e.g., [0052]; "a hole injection layer including an electron accepting compound and having a thickness of not more than 30 nm [i.e., including 30 nm, which is within the claimed range]"; see also Figure 2, there are two hole transporting layers, one on either side of the light emitting layer, and they are each of the thickness not more than 30 nm)**.**

Regarding claims 12, 20, 37 and 46, Kido and Nakaya disclose the inventions as explained above regarding claims 9, 13, 34 and 39 respectively, and Kido further discloses **t voltage is applied so as to make the light emitting element emit light, the electrode applied with higher potential is the first electrode, and the electrode applied with lower potential is the second electrode** (e.g., Figure 34 below, higher potential applied to first electrode, lower potential applied to second electrode, denoted by conventional circuitry)**.**

Fig. 34



Regarding claims 14 and 40, Kido and Nakaya disclose the inventions as explained above regarding claims 13 and 39 respectively, and Kido further discloses **the inorganic material (the P-type semiconductor; the material which accepts electrons) is a metal oxide** (e.g., [0033]; "the inorganic material can be a metal oxide")**.**

Regarding claims 15 and 41, Kido and Nakaya disclose the inventions as explained above regarding claims 13 and 39 respectively, and Kido further discloses **the metal oxide (the P-type semiconductor) is one or more compounds selected from the group consisting of vanadium oxide, molybdenum oxide, cobalt oxide, and nickel oxide, zinc oxide, indium oxide, tin oxide, antimony oxide, and tungsten oxide** (e.g., [0035]; "the metal oxide can be vandium pentaoxide")**.**

Regarding claims 16 and 42, Kido and Nakaya disclose the inventions as explained above regarding claims 13 and 39 respectively, and Kido further discloses **the N-type semiconductor is a metal oxide** (e.g., [0041]; "an electron injection layer [i.e., N-type semiconductor] having…a metal functioning as an electron donating dopant" and [0033]; "the inorganic material [i.e., the metal included in any of the charge generation layers] can be a metal oxide")**.**

Regarding claims 17 and 43, Kido and Nakaya disclose the inventions as explained above regarding claims 13 and 39 respectively, and Kido further discloses **the N-type semiconductor is one or more compounds selected from the group consisting of zinc oxide, zinc sulfide, zinc selenide, and titanium oxide** (e.g., [0033]; "the inorganic material [i.e., the metal in a charge generation layer] can be a metal oxide" and [0047]; "metal to include at least one selected from…titanium")**.**

Regarding claims 32, 33, 38 and 47, Kido and Nakaya teach the inventions as explained above regarding claims 9, 13, 34 and 39 respectively, and Nakaya further teaches **the light emitting element is incorporated in one selected from the group consisting of a television, a mobile phone, a computer, and a game machine** ([0227]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the light emitting device of Kido in a display device such as those listed in Nakaya, because OLEDs are suitable light emitting sources for the display devices listed in Nakaya.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARY ELLEN BOWMAN whose telephone number is (571) 270-5383. The examiner can normally be reached on Monday-Thursday, 7:30 a.m.-6:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. B./
Examiner, Art Unit 2879

/NIMESHKUMAR D. PATEL/
Supervisory Patent Examiner, Art Unit 2879